

FIGURE 1
(Prior Art)

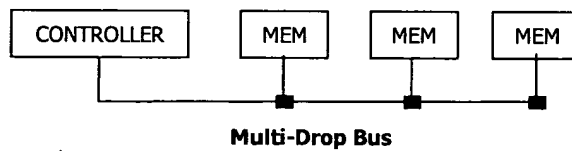


FIGURE 2
(Prior Art)

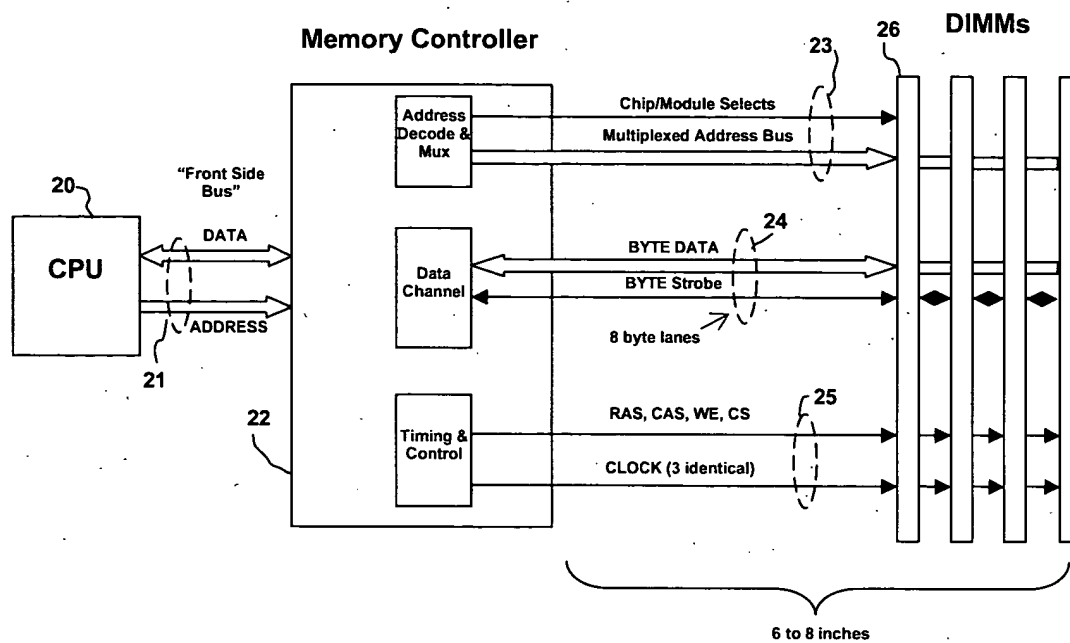


FIGURE 3

(Prior Art)

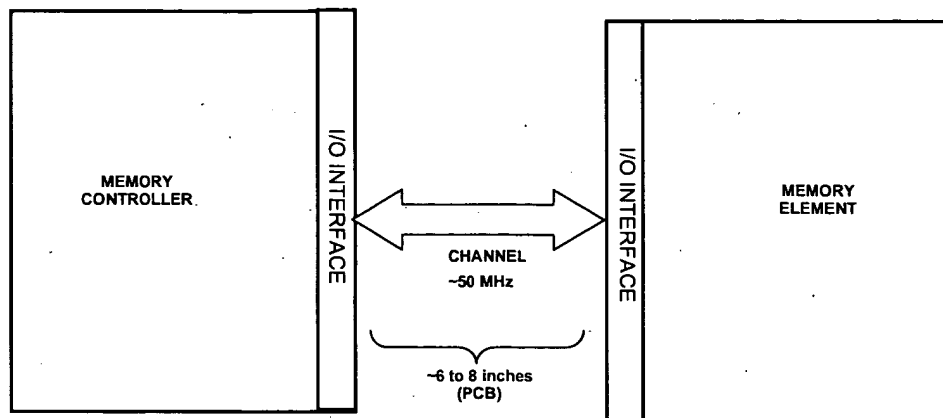


FIGURE 4

(Prior Art)

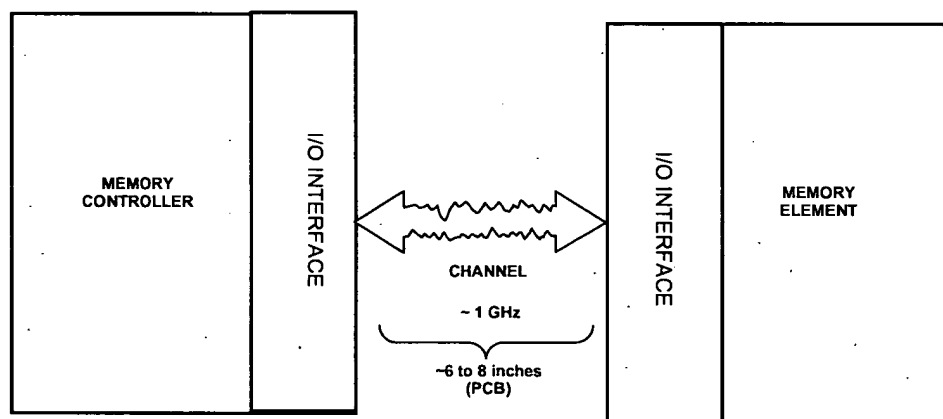


FIGURE 5

(Prior Art)

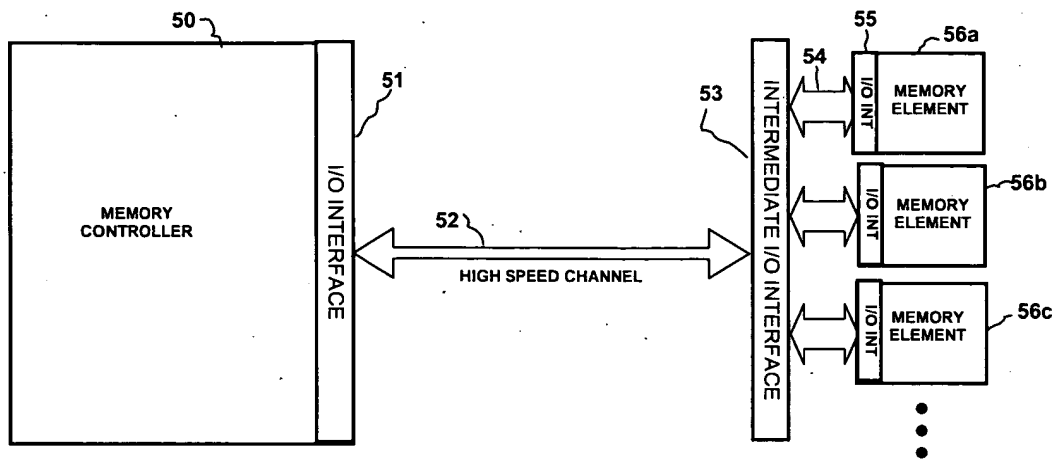


FIGURE 6

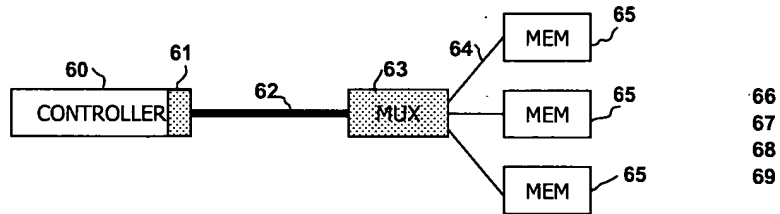


FIGURE 7

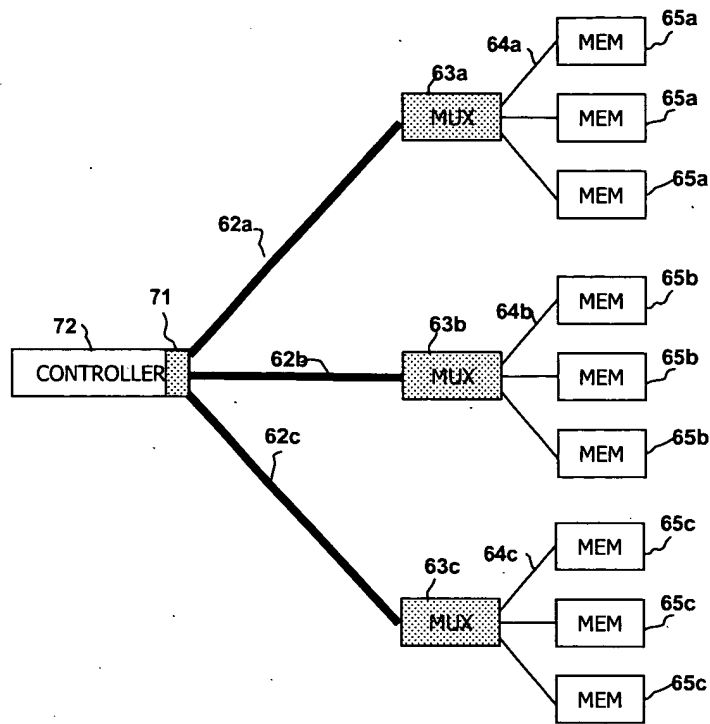


FIGURE 8

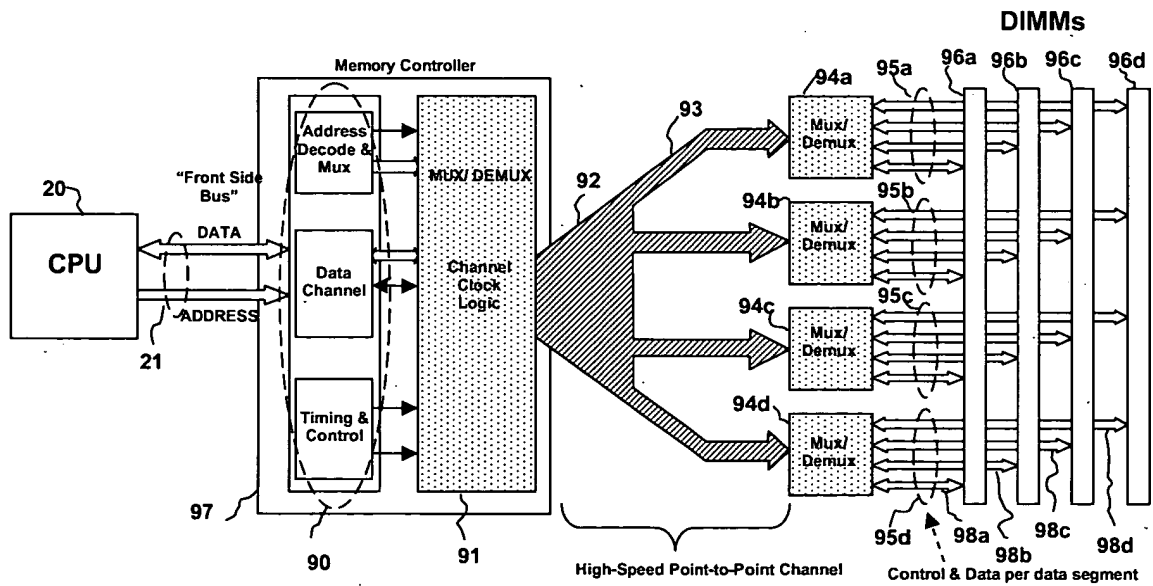


FIGURE 9

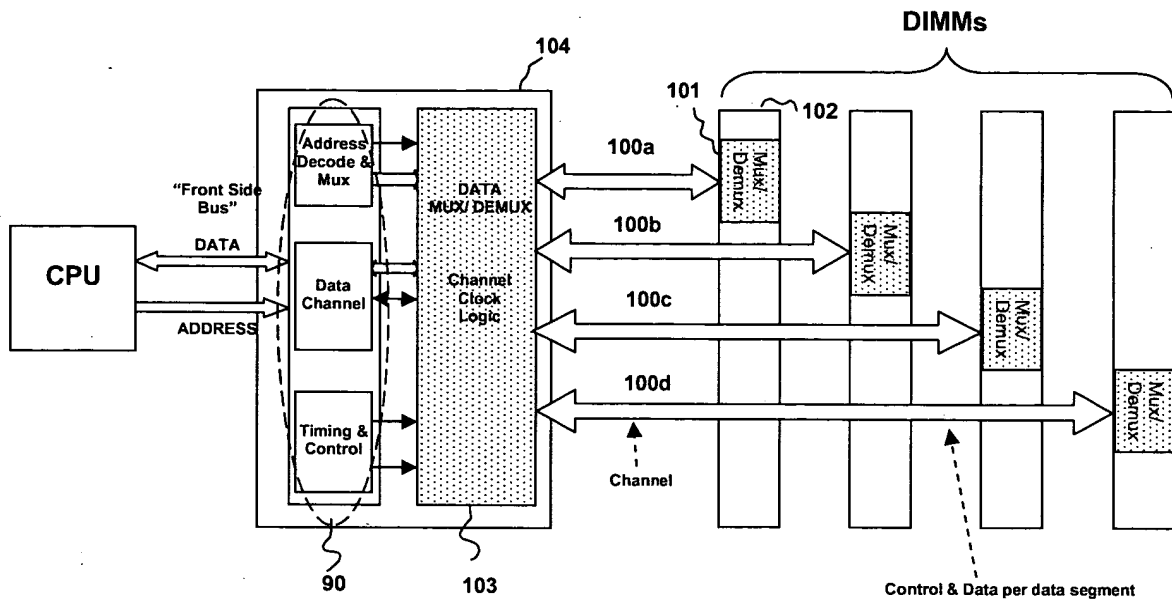


FIGURE 10

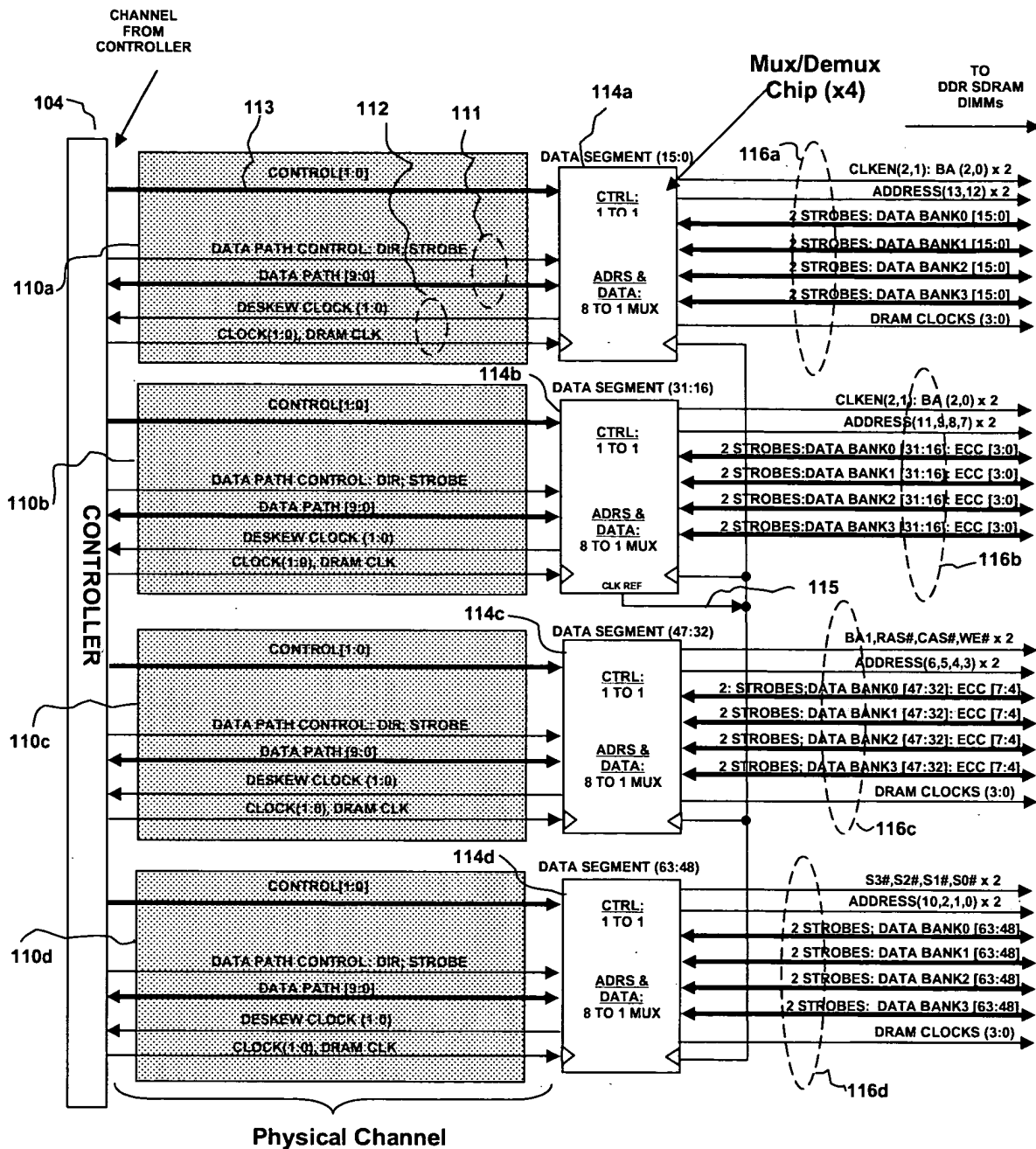


FIGURE 11

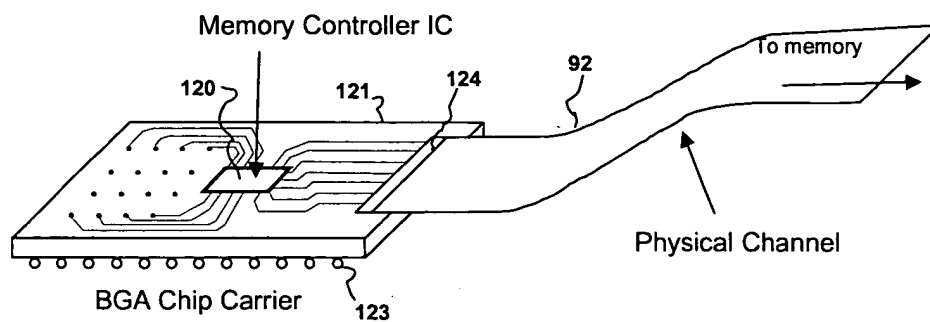


FIGURE 12

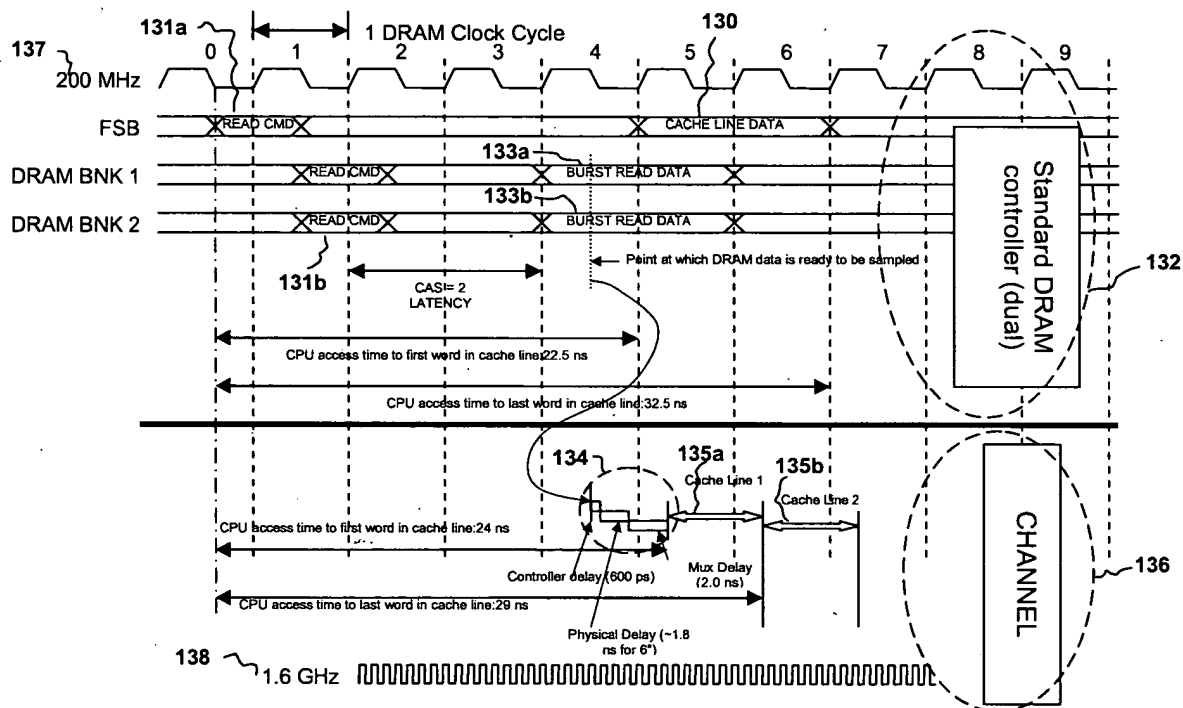


FIGURE 13

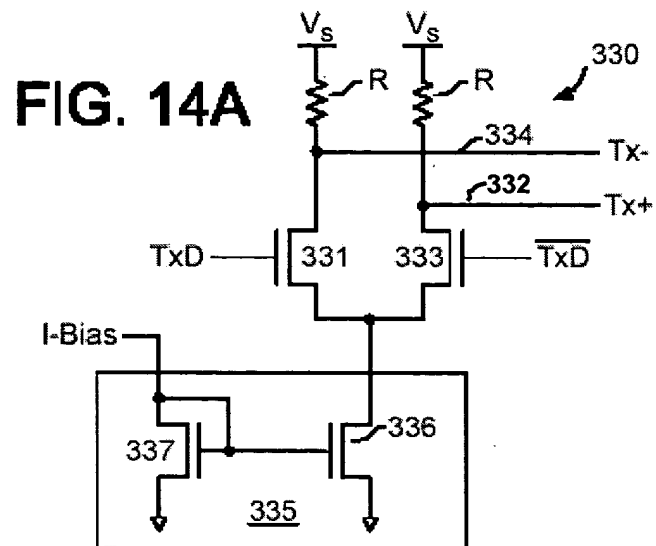


FIGURE 14A

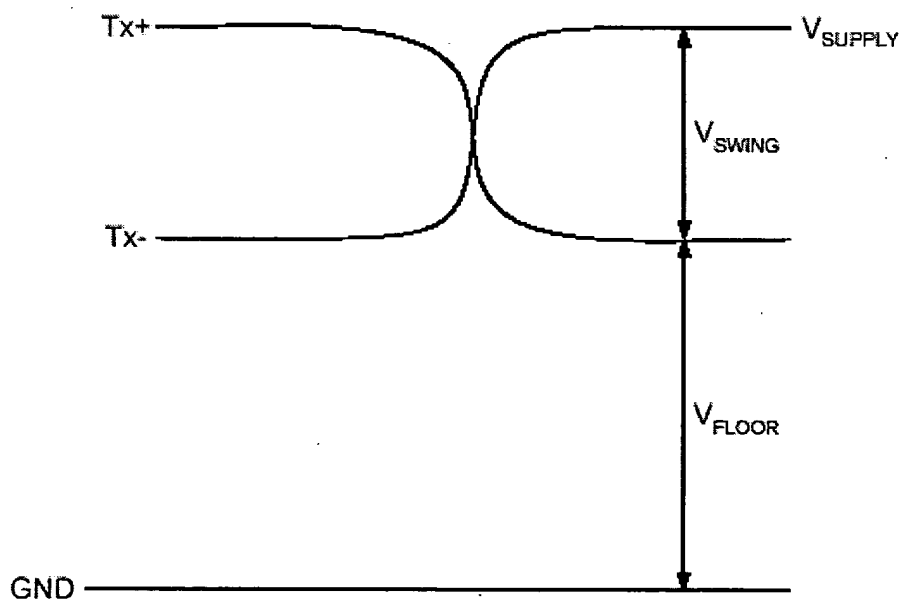


FIGURE 14B

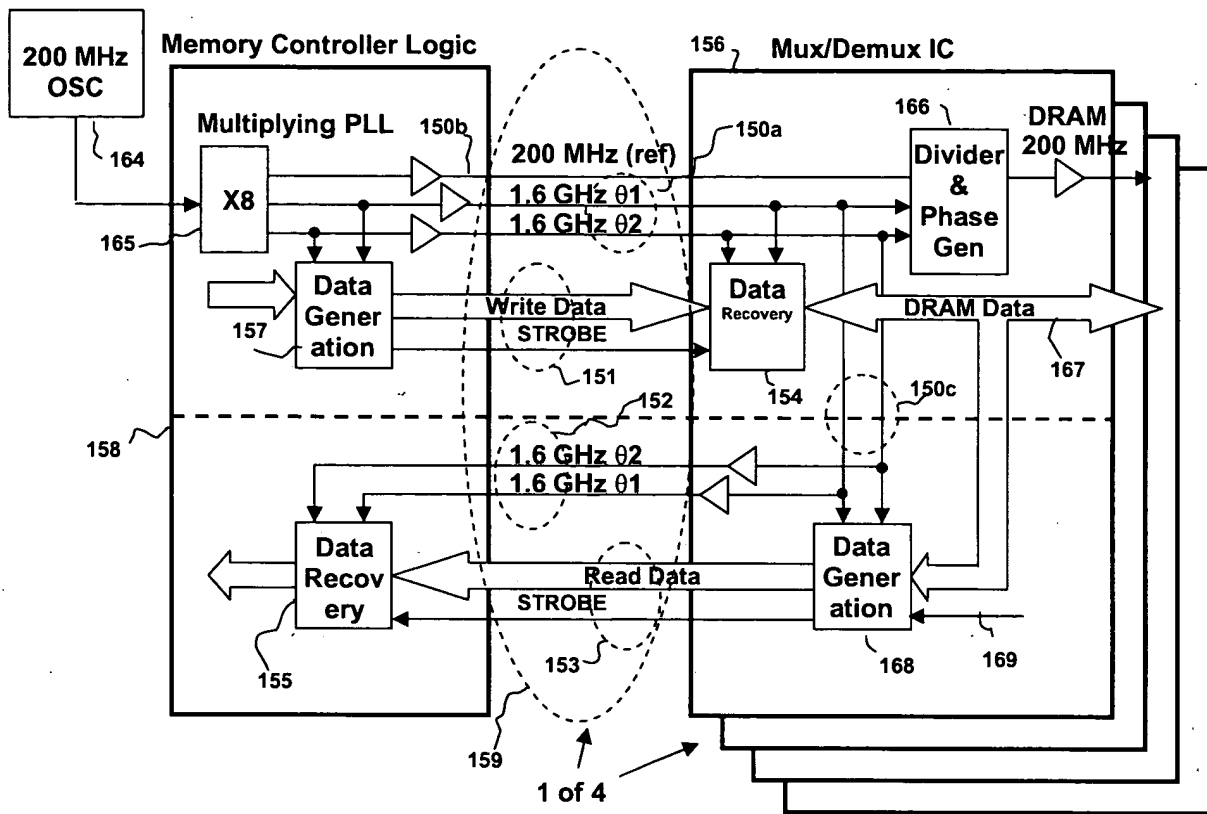


FIGURE 15

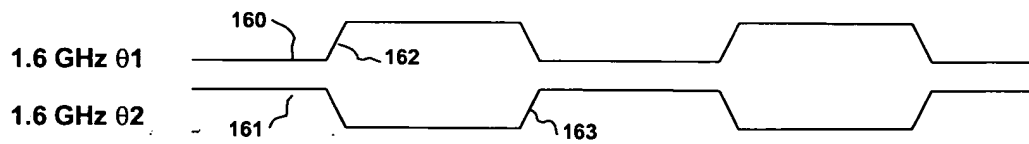


FIGURE 16

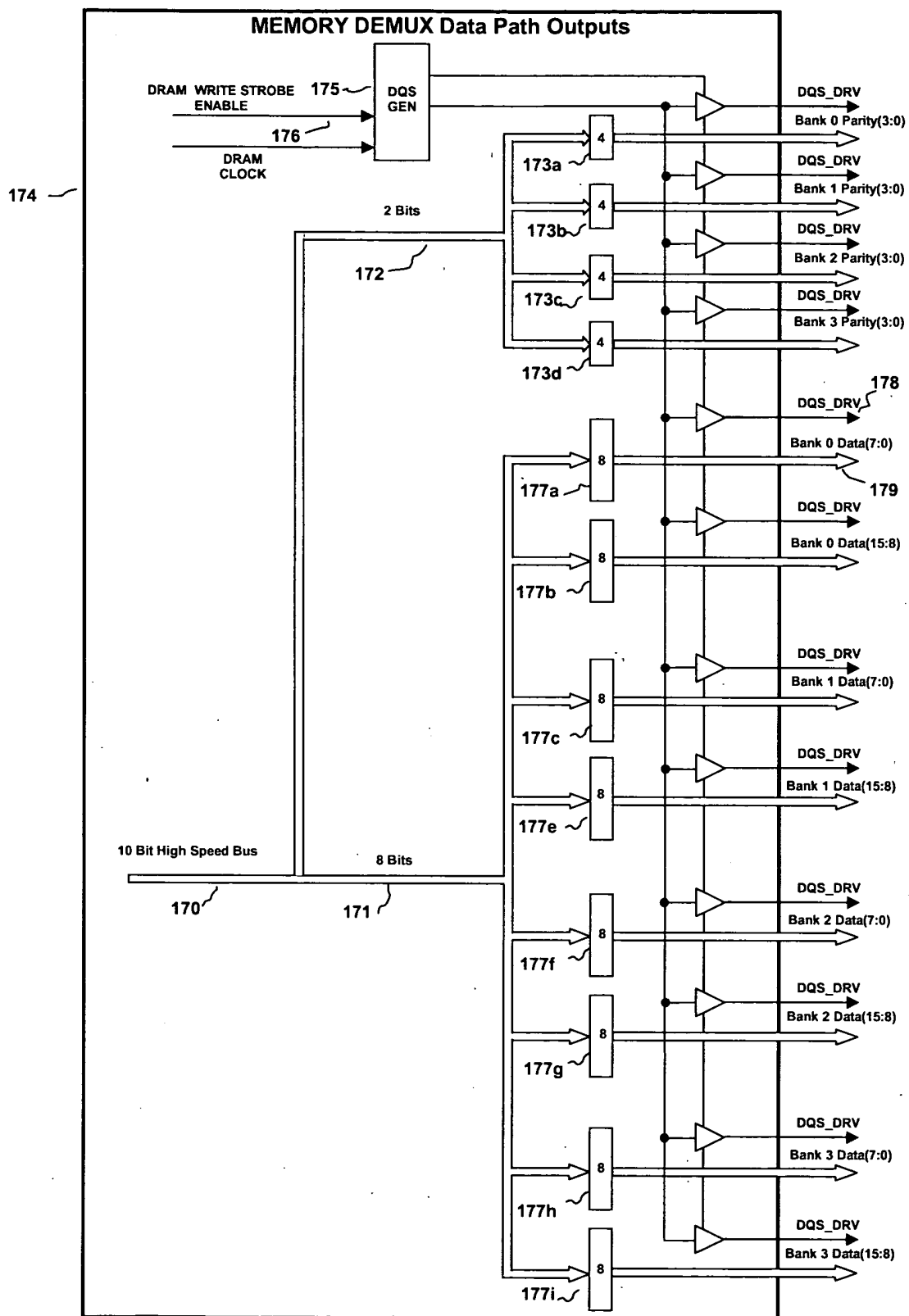


FIGURE 17

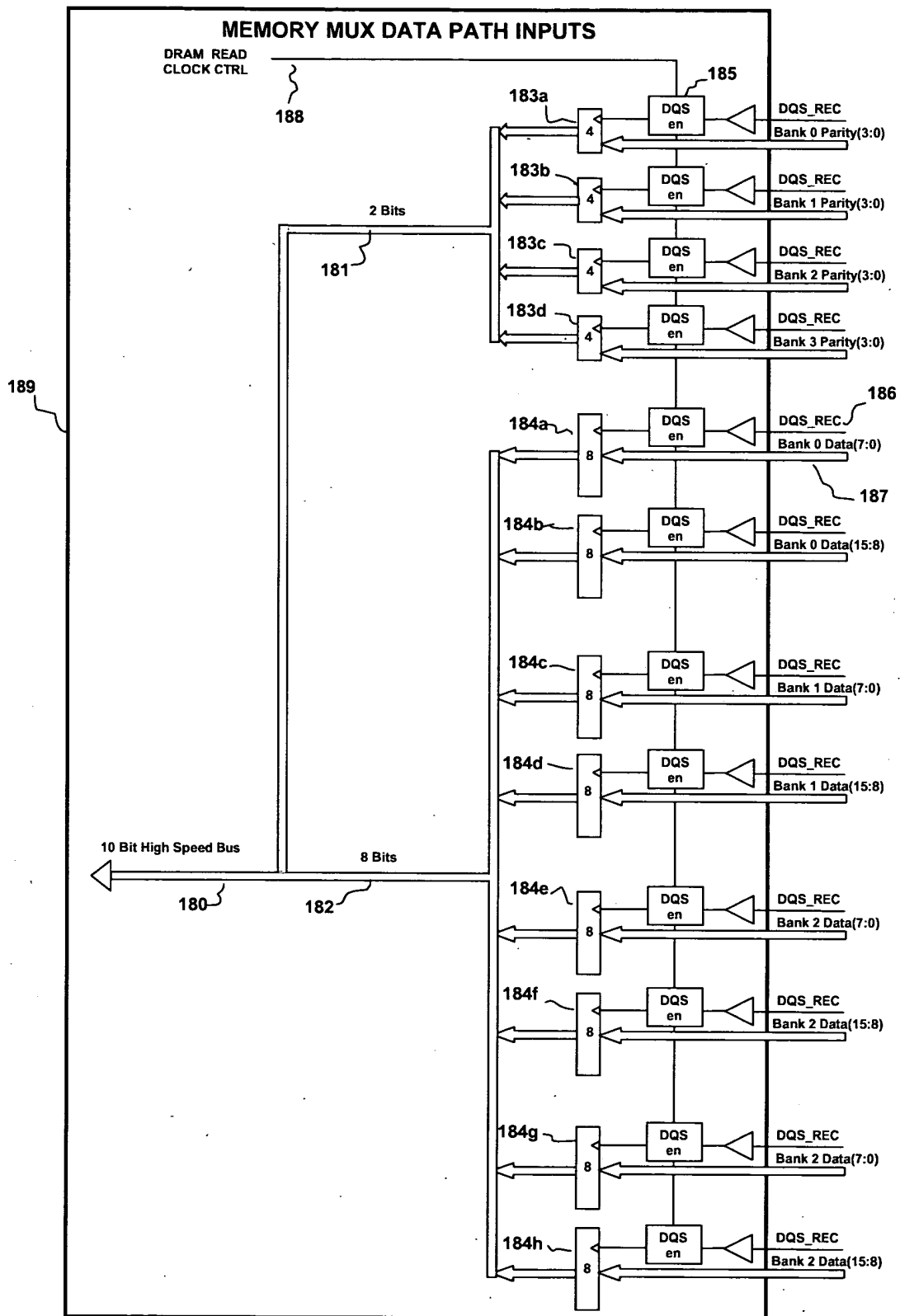


FIGURE 18

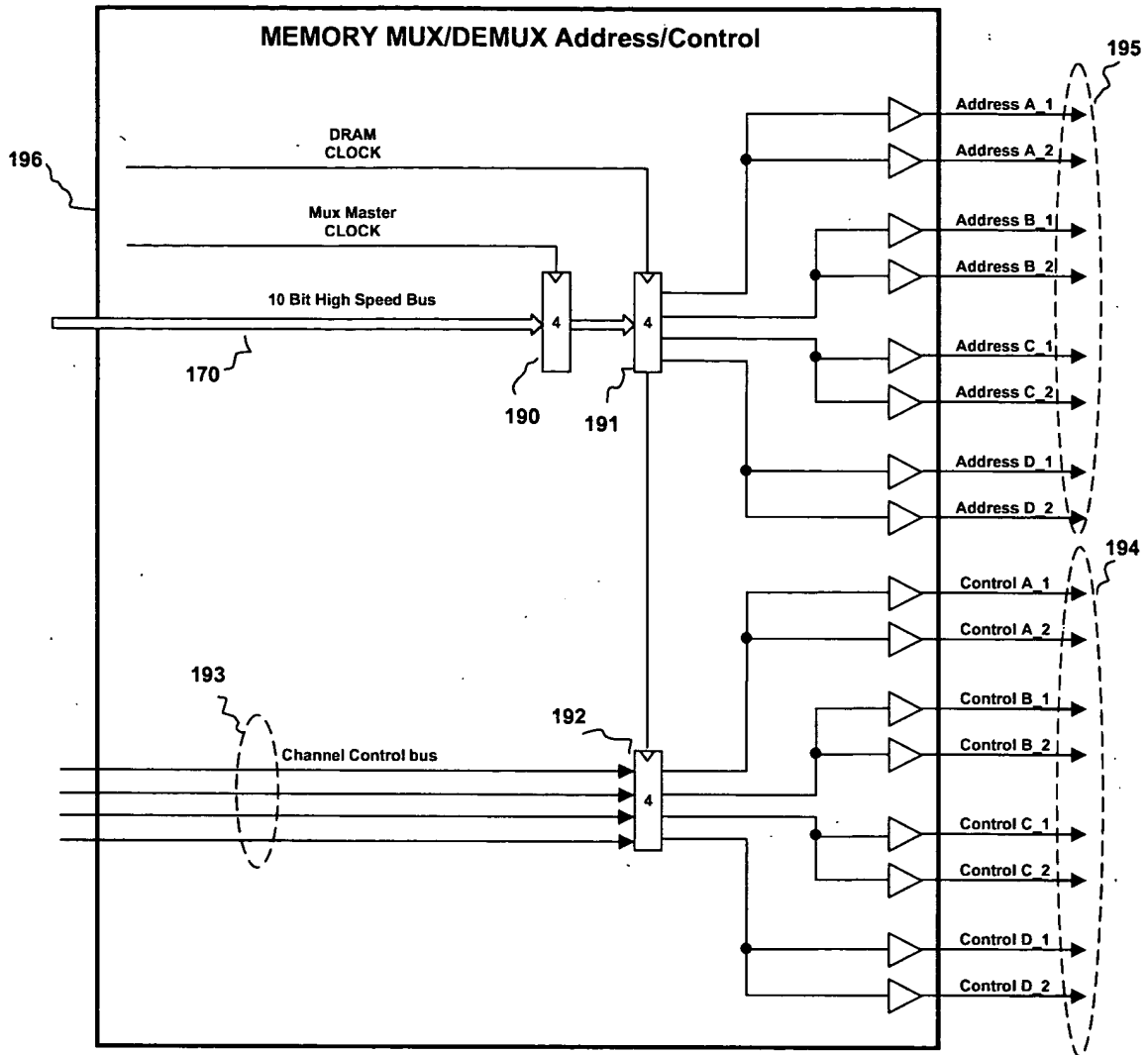


FIGURE 19

High-Speed Point-to-Point Channel Signals	Type	S or D	Pin Quan	DRAM Signals	Type	S or D	Pin Quan
Channel DATA	I/O	Dif	20	DRAM DATA	I/O	Sing	80
Channel CLK	I	Dif	2	DRAM CLOCK	O	Dif	8
Channel DESKEW CLK	O	Dif	2	DRAM REF CLK	O	Sin	2
Channel DRAM CLK	I	Dif	2	DRAM PLL CLK	I	Dif	2
Channel DIRECTION	I	Dif	2	DRAM STROBE	I/O	Sing	12
Channel STROBE ENABLE	I	Dif	2			Dif	
Channel CONTROL BUS	I	Dif	4	DRAM CONTROL	O	Sing	8
Channel Rev STROBE ENABLE	O	Dif	2	DRAM ADDRESS	O	Sing	8
Total			36	Total			120

FIGURE 20